REMARKS

Claims 1-20 are currently pending. In the February 8, 2008 Office Action, the Examiner objected to claims 18 and 19 for informalities, and claims 17 and 18 were rejected under 35 U.S.C. § 103(a) as unpatentable over Applicant's admission of prior art ("APA") in view of U.S. Patent No. 5,325,341 to Viot et al. ("Viot"). In addition, claims 1-16 were allowed, and the Examiner indicated that claims 19 and 20 would be allowable if rewritten to overcome the rejections and to include the base claim limitations. While Applicant appreciates the Examiner's indication of allowable subject matter and reserves the right to amend the claims as suggested by the Examiner, Applicant respectfully traverses the pending rejections of claims 17 and 18 for the reasons set forth hereinbelow.

A. Claims 18 and 19 Have Been Amended To Overcome The Objections

In response to the Examiner's objection to the noted informalities of claims 18 and 19, Applicant has amended the claims to correct the informalities as suggested by the Examiner, and to otherwise clarify the claims, and therefore requests that the objections be withdrawn.

A. Claims 17 and 18 Are Not Obvious over "Admitted Prior Art" and Viot

In response to the Examiner's rejection of claims 17 and 18 as being unpatentable over Viot, Applicant respectfully requests reconsideration and withdrawal of the rejection. Putting aside for the moment the propriety of combining the "admitted prior art" and Viot references or whether these references even qualify as prior art,[1] the proposed combination fails to disclose or make obvious the claimed scheme for generating time-out signals for a plurality of channels by running a free-running timer in a loop to generate a time-out signal/pulse "whenever a transition is observed in a first selected bit position of the free-running timer," as recited in claim 17. The Examiner's rejection analysis appears to assert that all of claim 17's requirements (except for the "single free-running timer" requirement) are met by "applicant's admission of prior art," and that Viot may be used to overcome this deficiency. However, this analysis appears to overstate the disclosure from "applicant's admission of prior art," and also mischaracterizes Viot's disclosed timer circuit.

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[1] In response to the Examiner's reliance on "admitted prior art," Applicant notes that everything described in the "Related Art" section of the present application is not necessarily "admitted prior art." Applicant expressly captioned the "Related Art" section, and did not describe this section as "Description of Prior Art." *See*, MPEP § 608.01(c) (The "Description of the Related Art" section may comprise a description of "other information disclosed known to the applicant, including references to … other information where appropriate.").

First of all, the Examiner asserts that "applicant's admission of prior art … teaches a method for generating time-out signals for a plurality of channels comprising the step of generating a first pulse when a first counter reaches a preset value, wherein the first pulse comprises a first time-out signal," citing paragraph 5 of Applicant's specification. Office Action, pp. 2-3. Applicant respectfully submits that the Examiner has mischaracterized the statement from Applicant's specification, since Applicant was actually describing the practice of using "multiple counter-based timers" to monitor multiple independent channels, where each counter generates a separate timer request "when the counter reaches zero (for count down counters) or a preset value":

> Conventional systems have used timing circuits to generate timing signals that are used in connection with the status monitoring functions and system operations. Such timing circuits typically are constructed with a counter that counts up or down, and when the counter reaches zero (for count down counters) or a preset value, a timer request is generated. When multiple counter-based timers are used for monitoring the status of multiple independent channels, the conventional timing circuit approach requires multiple counters that use significant chip area to provide a timer functionality for each channel. As the number of channels increases, the unwieldiness of conventional approaches also increases.

See, Application, paragraph 5 (emphasis added). Of particular significance is the description that the timer requests from each timing circuit are generated when the counter reaches zero (for count down counters) or a preset value. Thus, the "applicant's admission of prior art" does not disclose that time-out signals are generated "whenever a transition is observed in a first selected bit position of the free-running timer" as recited in claim 17.

This deficiency is not remedied by Viot's disclosure. In particular, the Examiner admits that the "applicant's admission of prior art" does not disclose using "a single free-running timer to generate said pulse" (Office Action, p. 3), but asserts that this admitted deficiency is remedied by Viot's disclosure of a "running a single free-running timer (12) in a loop … and generating a first pulse whenever a transition is observed in a first selected bit position of the timer," citing Viot, col. 3, line 34 to col. 4, line 14 and col. 6, lines 11-21. However, Applicant respectfully traverses this characterization of Viot's disclosure. Indeed, a careful reading of Viot confirms that Viot's "free running counter 12" uses a full bit comparison (when the counter is FFFF) before generating a pulse. This is shown in Viot Figure 2 where the counter 30 in the free running counter 12 generates "an active signal as its overflow output" when the up-counter 30 "reaches its full value (hexadecimal FFFF)." Viot, col. 5, line 58 to col. 6, line 21. In this respect, Viot's "free running counter 12" appears to be no more relevant than the conventional timing circuit approaches described in Applicant's Background of the Invention section. As a result, there is no disclosure or suggestion in Viot of generating a first time-out signal pulse "whenever a transition is observed in a first selected bit position of the free-running timer."

For at least the foregoing reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections because the Examiner has not made the *prima facie* obviousness showing that all the claim limitations are taught or suggested by the cited art. *See*, MPEP, § 2143.03 ("To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)."). Since the cited art fails to disclose "generating a first pulse **whenever a transition is observed in a first selected bit position of the free-running timer**, where said first pulse comprises a first time-out signal," Applicant respectfully submits that the obviousness rejection of claims 17-18 should be reconsidered and withdrawn, and that the claims should be allowed.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 338-9100.

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Respectfully submitted,

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